AD9516-3BCPZ

Clock Generator 0MHz to 250MHz-IN 2950MHz-OUT 64-Pin LFCSP EP Tray

Manufacturer:	Analog Devices, Inc
Package/Case:	QFN
Product Type:	Clock & Timer ICs
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The AD9516-3 emphasizes low jitter and phase noise to maximize data converter performance, and it can benefit other applications with demanding phase noise and jitter requirements.

The AD9516-3 features six LVPECL outputs (in three pairs) and four LVDS outputs (in two pairs). Each LVDS output can be reconfigured as two CMOS outputs. The LVPECL outputs operate to 1.6 GHz, the LVDS outputs operate to 800 MHz, and the CMOS outputs operate to 250 MHz.

Each pair of outputs has dividers that allow both the divide ratio and coarse delay (or phase) to be set. The range of division for the LVPECL outputs is 1 to 32. The LVDS/CMOS outputs allow a range of divisions up to a maximum of 1024.

The AD9516-3 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP) to 5 V. A separate LVPECL power supply can be from 2.5 V to 3.3 V (nominal).

The AD9516-3 is specified for operation over the standard industrial range of −40°C to +85°C.

Applications

Low jitter, low phase noise clock distribution
10/40/100 Gb/sec networking line cards, including SONET, Synchronous Ethernet, OTU2/3/4
Forward error correction (G.710)
Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
High performance wireless transceivers
ATE and high performance instrumentation

1 AD9516 is used throughout to refer to all the members of the AD9516 family. However, when AD9516-3 is used it is referring to that specific member of the AD9516 family.

Key Features

Low phase noise, phase-locked loop (PLL)-- On-chip VCO tunes from 1.75 GHz to 2.25 GHz-- External VCO/VCXO to 2.4 GHz optional-- 1 differential or 2 single-ended reference inputs

6 pairs of 1.6 GHz LVPECL outputs-- Each output pair shares a 1-to-32 divider with coarse phase delay-- Additive output jitter:225 fs rms-- Channel-to-channel skew paired outputs of <10 ps

4 pairs of 800 MHz LVDS clock outputs-- Each output pair shares two cascaded 1-to-32 dividers with coarse phase delay--Additive output jitter:275 fs rms

Automatic synchronization of all outputs on power-up

Manual output synchronization available

64-lead LFCSP

See datasheet for additional features

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Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs

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Recommended For You

AD9517-3ABCPZ

Analog Devices, Inc

QFN

AD9954YSV

Analog Devices, Inc

QFP

ADCLK914BCPZ-WP

Analog Devices, Inc

LFCSP-16

AD7008JP50

Analog Devices, Inc

PLCC44

AD9952YSV

Analog Devices, Inc

QFP

ADCLK944BCPZ-R2

Analog Devices, Inc

LFCSP16

AD9577BCPZ

Analog Devices, Inc

LFCSP-40

AD9543BCPZ

Analog Devices, Inc

LFCSP-48

AD9853AS

Analog Devices, Inc

QFP

ADN2805ACPZ

Analog Devices, Inc

LFCSP

AD9515BCPZ-REEL7

Analog Devices, Inc

LFCSP-32

ADN2807ACPZ

Analog Devices, Inc

48-LFCSP

AD9520-4BCPZ

Analog Devices, Inc

LFCSP

AD9831AST

Analog Devices, Inc

QFP

ADN2855ACPZ

Analog Devices, Inc

LFCSP32