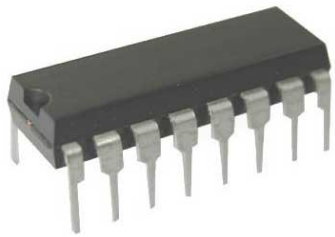
CD4021BE

Shift Register Single 8-Bit Serial/Parallel to Parallel 16-Pin PDIP Tube

Manufacturer:	Texas Instruments, Inc
Package/Case:	DIP16
Product Type:	Logic ICs
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active



Images are for reference only

Inquiry

General Description

CD4014B and CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is D-type, master-slave flip-flop. In addition to an output form stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock by parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

The CD4014B and CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix),16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes),and 16-lead thin shrink small-oultine packages (PW and PWR suffixes).

Key Features

Medium speed operation…12 MHz (typ.) clock rate at VDD – VSS = 10 V

Fully static operation

8 master-slave flip-flops plus output buffering and control gating

100% tested for quiescent current at 20 V

Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

Noise margin (full package-temperature range) = 1 V at VDD = 5 V 2 V at VDD = 10 V2.5 V at VDD = 15 V

Standardized, symmetrical output characteristics

5-V, 10-V, and 15-V parametric ratings

Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:
Parallel input/serial output data queueing

Parallel to serial data conversion

General-purpose register

Data sheet acquired from Harris Semiconductor
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Recommended For You

CD4070BE

Texas Instruments, Inc

DIP14

CD74HCT138E

Texas Instruments, Inc

DIP16

CD4098BE

Texas Instruments, Inc

DIP

CD74HC08E

Texas Instruments, Inc

DIP

CD74HC4075E

Texas Instruments, Inc

DIP

CD74ACT74E

Texas Instruments, Inc

DIP-14

CD74HC75E

Texas Instruments, Inc

DIP

CD4504BE

Texas Instruments, Inc

DIP16

CD4068BE

Texas Instruments, Inc

DIP

CD4081BE

Texas Instruments, Inc

DIP14

CD4001BE

Texas Instruments, Inc

DIP14

CD4512BE

Texas Instruments, Inc

DIP16

CD4069UBE

Texas Instruments, Inc

DIP14

CD74HCT151E

Texas Instruments, Inc

DIP

CD74HC04M

Texas Instruments, Inc

SOP14