CDCE906PW

Clock Generator 1MHz to 167MHz-IN 167MHz-OUT 20-Pin TSSOP Tube

Manufacturer:	Texas Instruments, Inc
Package/Case:	TSSOP20
Product Type:	Clock & Timer ICs
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The CDCE906 is one of the smallest and powerful PLL synthesizer / multiplier / divider available today. Despite its small physical outlines, the CDCE906 is flexible. It has the capability to produce an almost independent output frequency from a given input frequency.

The input frequency can be derived from a LVCMOS, differential input clock, or a single crystal. The appropriate input waveform can be selected via the SMBus data interface controller.

To achieve an independent output frequency the reference divider M and the feedback divider N for each PLL can be set to values from 1 up to 511 for the M-Divider and from 1 up to 4095 for the N-Divider. The PLL-VCO (voltage controlled oscillator) frequency than is routed to the free programmable output switching matrix to any of the six outputs. The switching matrix includes an additional 7-bit post-divider (1-to-127) and an inverting logic for each output. The deep M/N divider ratio allows the generation of zero ppm clocks from any reference input frequency (e.g., a 27 MHz).

The CDCE906 includes three PLLs of those one supports SSC (spread-spectrum clocking). PLL1, PLL2, and PLL3 are designed for frequencies up to 167 MHz and optimized for zero-ppm applications with wide divider factors.

PLL2 also supports center-spread and down-spread spectrum clocking (SSC). This is a common technique to reduce electro-magnetic interference. Also, the slew-rate controllable (SRC) output edges minimize EMI noise.

Based on the PLL frequency and the divider settings, the internal loop filter components will be automatically adjusted to achieve high stability and optimized jitter transfer characteristic of the PLL.

The device supports non-volatile EEPROM programming for easy-customized application. It is preprogrammed with a factory default configuration (see Figure 13) and can be reprogrammed to a different application configuration before it goes onto the PCB or reprogrammed by in-system programming. A different device setting is programmed via the serial SMBus interface.

Two free programmable inputs, S0 and S1, can be used to control for each application the most demanding logic control settings (outputs disable to low, outputs 3-state, power down, PLL bypass, etc).

The CDCE906 has three power supply pins, VCC, VCCOUT1 and VCCOUT2. VCC is the power supply for the device. It operates from a single 3.3-V supply voltage. VCCOUT1 and VCCOUT2 are the power supply pins for the outputs. VCCOUT1 supplies the outputs Y0 and Y1 and VCCOUT2 supplies the outputs Y2, Y3, Y4, and Y5. Both outputs supplies can be 2.3 V to 3.6 V. At output voltages lower than 3.3 V, the output drive current is limited.

The CDCE906 is characterized for operation from 0°C to 70°C.

Key Features

High Performance 3:6 PLL based Clock Synthesizer / Multiplier / Divider

User Programmable PLL Frequencies

EEPROM Programming Without the Need to Apply High Programming Voltage

Easy In-Circuit Programming via SMBus Data Interface

Wide PLL Divider Ratio Allows 0-ppm Output Clock Error

Generates Precise Video (27 MHz or 54 MHz) and Audio System Clocks from Multiple Sampling Frequencies (fS = 16, 22.05, 24, 32, 44.1, 48, 96 kHz)

Clock Inputs Accept a Crystal or a Single-Ended LVCMOS or a Differential Input Signal

Accepts Crystal Frequencies from 8 MHz up to 54 MHz

Accepts LVCMOS or Differential Input Frequencies up to 167 MHz

Two Programmable Control Inputs [S0/S1, A0/A1] for User Defined Control Signals

Six LVCMOS Outputs with Output Frequencies up to 167 MHz

LVCMOS Outputs can be Programmed for Complementary Signals

Free Selectable Output Frequency via Programmable Output Switching Matrix [6x6] Including 7-Bit Post-Divider for Each Output

PLL Loop Filter Components Integrated

Low Period Jitter (Typ 60 ps)

Programmable Center Spread SSC Modulation (±0.1%, ±0.25%, and ±0.4%) with a Mean Phase Equal to the Phase of the Non-Modulated Frequency

Programmable Down Spread SSC Modulation (1%, 1.5%, 2%, and 3%)

Programmable Output Slew-Rate Control (SRC) for Lowering System EMI

3.3-V Device Power Supply

Commercial Temperature Range 0°C to 70°C

Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock?)

Packaged in 20-Pin TSSOP

Recommended For You

CD4541BE

Texas Instruments, Inc

DIP14

CDCV304PW

Texas Instruments, Inc

TSSOP8

CDCV857ADGGR

Texas Instruments, Inc

TSSOP48

CDCV304PWR

Texas Instruments, Inc

TSSOP8

CDCVF2505PWR

Texas Instruments, Inc

TSSOP8

CDCE937PW

Texas Instruments, Inc

TSSOP20

CDCVF2310PWR

Texas Instruments, Inc

TSSOP24

CDCE62002RHBT

Texas Instruments, Inc

VQFN-32

CDCLVP110VF

Texas Instruments, Inc

QFP32

CDCLVD110ARHBT

Texas Instruments, Inc

VQFN-32

CDCDB803RSLR

Texas Instruments, Inc

VQFN-48

CDCP1803RGET

Texas Instruments, Inc

VQFN-24

CDCEL925PW

Texas Instruments, Inc

TSSOP16

CDCLVC1102PW

Texas Instruments, Inc

TSSOP8

CDCLVD1212RHAR

Texas Instruments, Inc

VQFN40