UART 2-CH 16byte FIFO 1.8V/2.5V/3.3V/5V 48-Pin TQFP Tray

Manufacturer:	Texas Instruments, Inc
Package/Case:	QFP
Product Type:	Drivers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The TL16C2550 is a dual universal asynchronous receiver and transmitter (UART). It incorporates the functionality of two TL16C550D UARTs, each UART having its own register set and FIFOs. The two UARTs share only the data bus interface and clock source, otherwise they operate independently. Another name for the uart function is Asynchronous Communications Element (ACE), and these terms will be used interchangeably. The bulk of this document describes the behavior of each ACE, with the understanding that two such devices are incorporated into the TL16C2550.

Each ACE is a speed and voltage range upgrade of the TL16C550C, which in turn is a functional upgrade of the TL16C450. Functionally equivalent to the TL16C450 on power up or reset (single character or TL16C450 mode), each ACE can be placed in an alternate FIFO mode. This relieves the CPU of excessive software overhead by buffering received and to be transmitted characters. Each receiver and transmitter store up to 16 bytes in their respective FIFOs, with the receive FIFO including three additional bits per byte for error status. In the FIFO mode, a selectable autoflow control feature can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using handshakes between the RTS output and CTS input, thus eliminating overruns in the receive FIFO.

Each ACE performs serial-to-parallel conversions on data received from a peripheral device or modem and stores the parallel data in its receive buffer or FIFO, and each ACE performs parallel-to-serial conversions on data sent from its CPU after storing the parallel data in its transmit buffer or FIFO. The CPU can read the status of either ACE at any time. Each ACE includes complete modem control capability and a processor interrupt system that can be tailored to the application.

Each ACE includes a programmable baud rate generator capable of dividing a reference clock with divisors from 1 to 65535, thus producing a 16× internal reference clock for the transmitter and receiver logic. Each ACE accommodates up to a 1.5-Mbaud serial data rate (24-MHz input clock). As a reference point, that speed would generate a 667-ns bit time and a 6.7-μs character time (for 8,N,1 serial data), with the internal clock running at 24 MHz.

Each ACE has a TXRDY and RXRDY output that can be used to interface to a DMA controller.

Key Features

Programmable Auto-RTS and Auto-CTS

In Auto-CTS Mode, CTS Controls Transmitter

In Auto-RTS Mode, RCV FIFO Contents, and Threshold Control RTS

Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment Is on the Same Power Drop

Capable of Running With All Existing TL16C450 Software

After Reset, All Registers Are Identical to the TL16C450 Register Set

Up to 24-MHz Clock Rate for up to 1.5-Mbaud Operation With VCC = 5 V

Up to 20-MHz Clock Rate for up to 1.25-Mbaud Operation With VCC = 3.3 V

Up to 16-MHz Clock Rate for up to 1-Mbaud Operation With VCC = 2.5 V

Up to 10-MHz Clock Rate for up to 625-kbaud Operation With VCC = 1.8 V

In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data

Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2 16 -1) and Generates an Internal 16 × Clock

Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream

5-V, 3.3-V, 2.5-V, and 1.8-V Operation

Independent Receiver Clock Input

Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled

Fully Programmable Serial Interface Characteristics:
5-, 6-, 7-, or 8-Bit Characters

Even-, Odd-, or No-Parity Bit Generation and Detection

1-, 1 1/2-, or 2-Stop Bit Generation

Baud Generation (DC to 1 Mbit/s)

False-Start Bit Detection

Complete Status Reporting Capabilities

3-State Output TTL Drive Capabilities for Bidirectional Data Bus and Control Bus

Line Break Generation and Detection Internal Diagnostic Capabilities:
Loopback Controls for Communications Link Fault Isolation

Break, Parity, Overrun, and Framing Error Simulation

Fully Prioritized Interrupt System Controls

Modem Control Functions (CTS, RTS, DSR, DTR, RI, and DCD)

Available in 48-Pin TQFP (PFB) Package, 32-Pin QFN (RHB), or 44-Pin PLCC (FN) Package

Pin Compatible with TL16C752B (48-Pin Package PFB)

Recommended For You

TLV320AIC23BIPWR

Texas Instruments, Inc

TSSOP28

TLV320AIC3104IRHBR

Texas Instruments, Inc

QFN32

TL16C554AIPN

Texas Instruments, Inc

LQFP80

TLV320AIC3101IRHBR

Texas Instruments, Inc

QFN32

TL16C554APN

Texas Instruments, Inc

LQFP80

TLV320AIC24KIPFBR

Texas Instruments, Inc

TQFP-48

TL16C554PN

Texas Instruments, Inc

QFP

TLV320AIC24KIPFB

Texas Instruments, Inc

TQFP-48

TL16C752BLPTREP

Texas Instruments, Inc

LQFP-48

TL16C550DIPFBR

Texas Instruments, Inc

48-TQFP

TLC320AC01CFN

Texas Instruments, Inc

PLCC28

TL16C552AFN

Texas Instruments, Inc

PLCC

TL16C450FN

Texas Instruments, Inc

PLCC44

TL16C554FN

Texas Instruments, Inc

PLCC

TLV320AIC31IRHBR

Texas Instruments, Inc

VQFN32