TSB41AB2PAP

Two Port Cable Transceiver/Arbiter 1TX 1RX 400Mbps 64-Pin HTQFP EP Tray

Manufacturer:	Texas Instruments, Inc
Package/Case:	QFP
Product Type:	Discrete Semiconductor Modules
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The TSB41AB2 provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based IEEE 1394 network. The cable ports incorporate two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41AB2 is designed to interface with a link layer controller (LLC), such as the TSB12LV21, TSB12LV22, TSB12LV23, TSB12LV26, TSB12LV31, TSB12LV41, TSB12LV42, or TSB12LV01A.

The TSB41AB2 requires only an external 24.576-MHz crystal as a reference. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

The TSB41AB2 supports an optional isolation barrier between itself and its LLC. When the ISO\ input terminal is tied high, the LLC interface outputs behave normally. When the ISO\ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in Annex J of IEEE Std 1394-1995 and in IEEE 1394a-2000 (section 5.9.4) (hereinafter referred to as Annex J type isolation). To operate with TI bus holder isolation, the ISO\ terminal on the PHY must be high.

Data bits to be transmitted through the cable ports are received from the LLC on two, four, or eight parallel paths (depending on the requested transmission speed) and are latched internally in the TSB41AB2 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 393.216 Mbits/s (referred to as S100, S200, and S400 speed respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two-, four-, or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152-MHz system clock and sent to the associated LLC.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB41AB2 provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 µF. TPBIAS is close to VDD when an active port is not connected to another node.

The line drivers in the TSB41AB2 operate in a high-impedance current mode, and are designed to work with external 112- ±1.0%.

When the power supply of the TSB41AB2 is off while the twisted-pair cables are connected, the TSB41AB2 transmitter and receiver circuitry presents a high

impedance to the cable and does not load the TPBIAS voltage at the other end of the cable. Fail-safe circuitry blocks any leakage path from the port back to the device power plane.

When the TSB41AB2 is used with one of the ports not brought out to a connector, the twisted-pair terminals of the unused port must be terminated for reliable operation. For each unused port, the TPB+ and TPB– terminals should be tied together and then pulled to ground, or the TPB+ and TPB– terminals should be connected to the suggested termination network (see Figure 5). The TPA+ and TPA– and TPBIAS terminals of an unused port may be left unconnected. The TPBIAS terminal should be connected to a 1-μF capacitor to ground or left floating.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal should be connected to VDD through a 1-k resistor, and SM should be connected directly to ground.

Four package terminals are used as inputs to set the default value for four configuration status bits in the self-ID packet, and are tied high through a 1-k resistor or hardwired low as a function of the equipment design. The PC0–PC2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 9 for power-class encoding. The C/LKON terminal is used as an input to indicate that the node is a contender for either isochronous resource manager (IRM) or bus manager (BM).

The TSB41AB2 supports suspend/resume as defined in IEEE 1394a-2000 specification. The suspend mechanism allows pairs of directly-connected ports to be placed into a low-power state (suspended state) while maintaining a port-to-port connection between bus segments. While in the suspended state, a port is unable to transmit or receive data transaction packets. However, a port in the suspended state is capable of detecting connection status changes and detecting incoming TPBIAS. When ports of the TSB41AB2 are suspended, all circuits except the band gap reference generator and bias detection circuits are powered down, resulting in significant power savings. For additional details of suspend/resume operation see IEEE 1394a-2000. The use of suspend/resume is recommended for new designs.

The port transmitter and receiver circuitry is disabled during power down (when the PD input terminal is asserted high), during reset (when the RESET\ input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The TPBIAS output is disabled during power down, during reset, or when the port is disabled as commanded by the LLC.

The cable-not-active (CNA) output terminal is asserted high when there are no twisted-pair cable ports receiving incoming bias (that is, they are either disconnected or suspended), and can be used along with LPS to determine when to power down the TSB41AB2. The CNA output is not debounced. When the PD terminal is asserted high, the CNA detection circuitry is enabled (regardless of the previous state of the ports) and a pulldown is activated on the RESET\ terminal to force a reset of the TSB41AB2 internal logic.

The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used in conjunction with the LCtrl bit (see Table 1 and Table 2 in the Application Information section) to indicate the active/power status of the LLC. The LPS signal is also used to reset, disable, and initialize the PHY-LLC interface (the state of the PHY-LLC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

The LPS input is considered inactive if it remains low for more than 2.6 μs and is considered active otherwise. When the TSB41AB2 detects that LPS is inactive, it places the PHY-LLC interface into a low-power reset state in which the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs, the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is also held in the disabled state during hardware reset. The TSB41AB2 continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY initializes the interface and returns it to normal operation.

When the PHY-LLC interface is in the low-power disabled state, the TSB41AB2 automatically enters a low-power mode if the port is inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB41AB2 disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the port (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the ultralow-power sleep mode) is attained when the port is either disconnected, or disabled with the port interrupt enable bit cleared. The TSB41AB2 exits the low-power mode when the LPS input is asserted high or when a port event occurs. This requires that the TSB41AB2 become active in order to respond to the event or to notify the LLC of the event (for example, incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The SYSCLK output becomes active (and the PHY-LLC interface is initialized and become operative) within 7.3 ms after LPS is asserted high when the TSB41AB2 is in the low-power mode.

The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163-ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts the C/LKON output when a bus reset occurs unless a PHY interrupt condition exists which would otherwise cause C/LKON to be active.

Key Features

Fully compliant with open HCI requirements

Extended resume signalling for compatibility

Power-down features to conserve energy in battery powered applications

Automatic device power down during suspend

Device power-down terminal

Software device reset (SWR)

Industry leading low power consumption

Ultralow-power sleep mode

Cable power presence monitoring

Cable ports monitor line conditions for active connection to remote node

Interoperable with link layer controllers using 3.3V

Single-supply operation

Green product and no Sb/Br

Recommended For You

DS25BR150TSD/NOPB

Texas Instruments, Inc

WSON8

TSB12LV32PZ

Texas Instruments, Inc

TQFP100

TSB81BA3DPFP

Texas Instruments, Inc

HTQFP80

TSB41AB1PHP

Texas Instruments, Inc

QFP48

TSB43CB43APGF

Texas Instruments, Inc

176-LQFP

DS25BR100TSD/NOPB

Texas Instruments, Inc

WSON-8

TSB12LV26PZT

Texas Instruments, Inc

QFP100

DS25BR110TSD/NOPB

Texas Instruments, Inc

WSON8

TSB43AB21AIPDTEP

Texas Instruments, Inc

TQFP128

DS15BR401TSQ/NOPB

Texas Instruments, Inc

QFN

TSB81BA3PFP

Texas Instruments, Inc

QFP

TS5USBC410IYFFR

Texas Instruments, Inc

DSBGA-12

TSB43DA42GHC

Texas Instruments, Inc

BGA

TS5USBC412YFFR

Texas Instruments, Inc

DSBGA-12

DS99R104TSQX/NOPB

Texas Instruments, Inc

LLP