

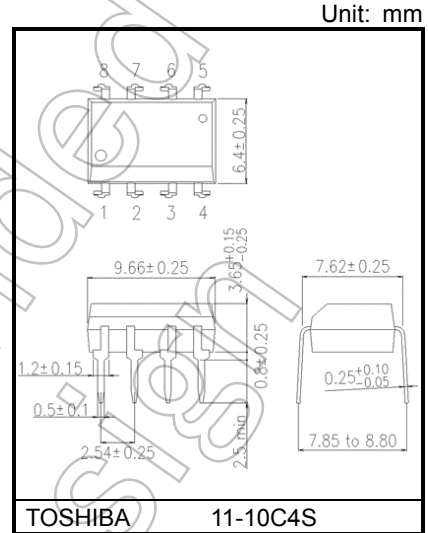
TLP250

Industrial Inverter
 Inverter For Air Conditioner
 IGBT Gate Drive
 Power MOS FET Gate Drive

The TOSHIBA TLP250 consists of an infrared emitting diode and a integrated photodetector.
 This unit is 8-lead DIP package.
 TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: 5mA(max)
- Supply current : 11mA(max)
- Supply voltage : 10-35V
- Output current : $\pm 1.5A$ (max)
- Switching time t_{pLH}/t_{pHL} : 0.5 μ s(max)
- Isolation voltage: 2500V_{rms}(min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-Approved: EN 60747-5- 5 (Note 1)

Note 1: When a VDE approved type is needed, please designate the **Option(D4)**.

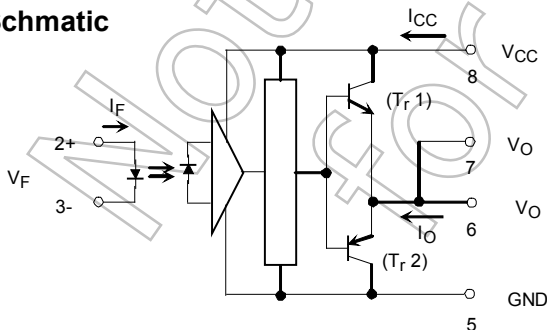


Weight: 0.54 g (typ.)

Truth Table

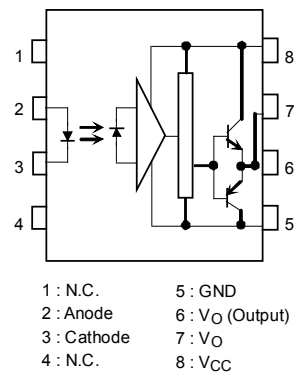
		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

Schematic



A 0.1 μ F bypass capacitor must be connected between pin 8 and 5

Pin Configuration (top view)



Start of commercial production
 1990-11

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
LED	Forward current	I_F	20	mA	
	Forward current derating (Ta ≥ 70°C)	$\Delta I_F / \Delta T_a$	-0.36	mA / °C	
	Peak transient forward current (Note 1)	I_{FPT}	1	A	
	Reverse voltage	V_R	5	V	
	Diode power dissipation	P_D	40	mW	
	Diode power dissipation derating (Ta ≥ 70°C)	$\Delta P_D / ^\circ C$	-0.72	mW / °C	
	Junction temperature	T_j	125	°C	
Detector	"H" peak output current ($P_W \leq 2.5\mu s, f \leq 15kHz$) (Note 2)	I_{OPH}	-1.5	A	
	"L" peak output current ($P_W \leq 2.5\mu s, f \leq 15kHz$) (Note 2)	I_{OPL}	+1.5	A	
	Output voltage	(Ta ≤ 70°C)	V_O	35	V
		(Ta ≤ 85°C)		24	
	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
		(Ta ≤ 85°C)		24	
	Output voltage derating (Ta ≥ 70°C)	$\Delta V_O / \Delta T_a$	-0.73	V / °C	
	Supply voltage derating (Ta ≥ 70°C)	$\Delta V_{CC} / \Delta T_a$	-0.73	V / °C	
	Power dissipation	P_C	800	mW	
	Power dissipation derating (Ta ≥ 70°C)	$\Delta P_C / ^\circ C$	-14.5	mW / °C	
	Junction temperature	T_j	125	°C	
Operating frequency (Note 3)	f	25	kHz		
Operating temperature range	T_{opr}	-20 to 85	°C		
Storage temperature range	T_{stg}	-55 to 125	°C		
Lead soldering temperature (10 s)	T_{sol}	260	°C		
Isolation voltage (AC, 60 s., R.H. ≤ 60 %) (Note 4)	BV_S	2500	Vrms		

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width $P_W \leq 1 \mu s$, 300 pps

Note 2: Exponential waveform

Note 3: Exponential waveform, $I_{OPH} \leq -1.0 A (\leq 2.5 \mu s)$, $I_{OPL} \leq +1.0 A (\leq 2.5 \mu s)$

Note 4: Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, on	$I_{F(ON)}$	7	8	10	mA
Input voltage, off	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage	V_{CC}	15	—	30	V
Peak output current	I_{OPH}/I_{OPL}	—	—	±0.5	A
Operating temperature	T_{opr}	-20	25	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note : A ceramic capacitor(0.1 μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note : Input signal rise time(fall time)<0.5 μs.

Electrical Characteristics (Ta = -20 to 70°C, unless otherwise specified)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Input forward voltage		V _F	—	I _F = 10 mA, Ta = 25 °C	—	1.6	1.8	V	
Temperature coefficient of forward voltage		ΔV _F / ΔTa	—	I _F = 10 mA	—	-2.0	—	mV / °C	
Input reverse current		I _R	—	V _R = 5 V, Ta = 25 °C	—	—	10	μA	
Input capacitance		C _T	—	V = 0 V, f = 1 MHz, Ta = 25 °C	—	45	250	pF	
Output current	"H" level	I _{OPH}	1	V _{CC} = 30 V (Note 1)	I _F = 10 mA V ₈₋₆ = 4 V	-0.5	-1.5	—	A
	"L" level	I _{OPL}	2		I _F = 0 mA V ₆₋₅ = 2.5 V	0.5	2	—	
Output voltage	"H" level	V _{OH}	3	V _{CC1} = +15 V, V _{EE1} = -15 V R _L = 200 Ω, I _F = 5 mA	11	12.8	—	V	
	"L" level	V _{OL}	4	V _{CC1} = +15 V, V _{EE1} = -15 V R _L = 200 Ω, V _F = 0.8 V	—	-14.2	-12.5		
Supply current	"H" level	I _{CCH}	—	V _{CC} = 30 V, I _F = 10 mA Ta = 25 °C	—	7	—	mA	
				V _{CC} = 30 V, I _F = 10 mA	—	—	11		
	"L" level	I _{CCL}	—	V _{CC} = 30 V, I _F = 0 mA Ta = 25 °C	—	7.5	—		
				V _{CC} = 30 V, I _F = 0 mA	—	—	11		
Threshold input current	"Output L→H"	I _{FLH}	—	V _{CC1} = +15 V, V _{EE1} = -15 V R _L = 200 Ω, V _O > 0 V	—	1.2	5	mA	
Threshold input voltage	"Output H→L"	V _{FHL}	—	V _{CC1} = +15 V, V _{EE1} = -15 V R _L = 200 Ω, V _O < 0 V	0.8	—	—	V	
Supply voltage		V _{CC}	—	—	10	—	35	V	
Capacitance (input-output)		C _S	—	V _S = 0 V, f = 1 MHz Ta = 25 °C	—	1.0	2.0	pF	
Resistance(input-output)		R _S	—	V _S = 500 V, Ta = 25 °C R.H. ≤ 60 %	1×10 ¹²	10 ¹⁴	—	Ω	

* All typical values are at Ta = 25°C

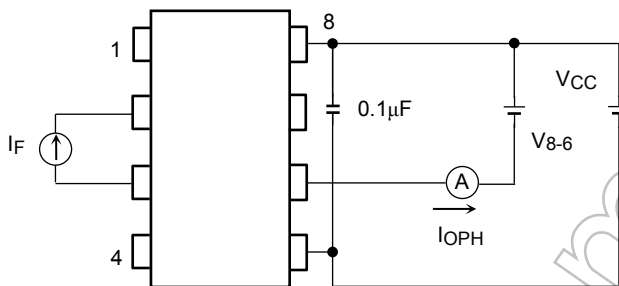
Note 1: Duration of I_O time ≤ 50μs

Switching Characteristics (Ta = -20 to 70°C, unless otherwise specified)

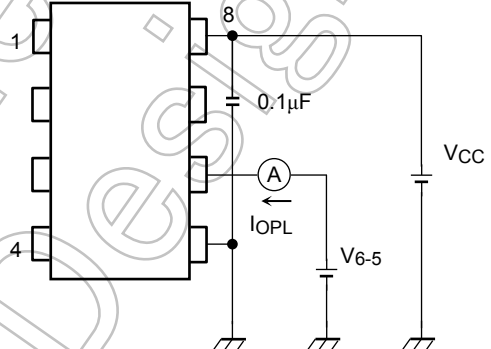
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time	L→H	5	I _F = 8 mA V _{CC1} = +15 V, V _{EE1} = -15 V R _L = 200 Ω	—	0.15	0.5	μs
	H→L			—	0.15	0.5	
Common mode transient immunity at high level output	CMH	6	V _{CM} = 600 V, I _F = 8 mA V _{CC} = 30 V, Ta = 25 °C	-5000	—	—	V / μs
Common mode transient immunity at low level output	CM _L		V _{CM} = 600 V, I _F = 0 mA V _{CC} = 30 V, Ta = 25 °C	5000	—	—	V / μs

Note: All typical values are at Ta = 25°C

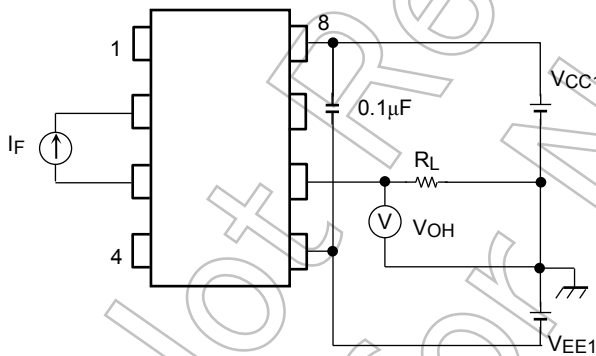
Test Circuit 1 : I_{OPH}



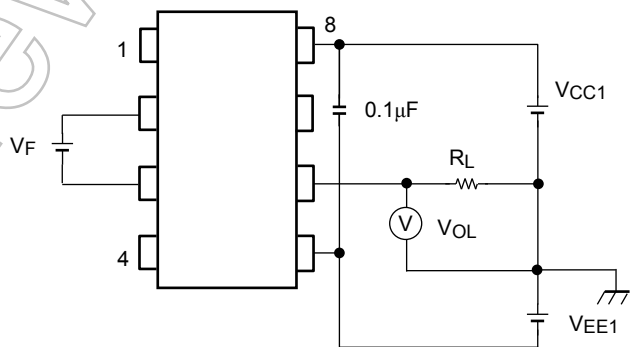
Test Circuit 2 : I_{OPL}



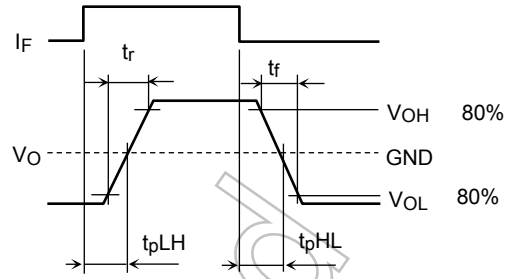
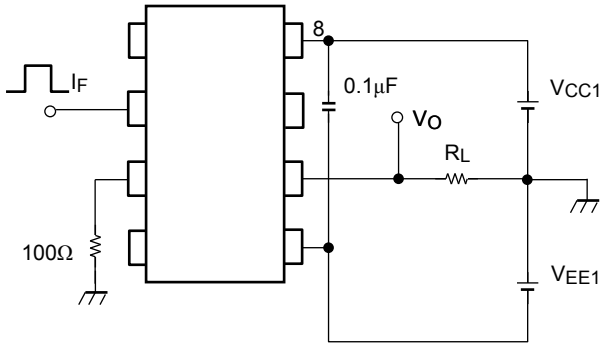
Test Circuit 3 : V_{OH}



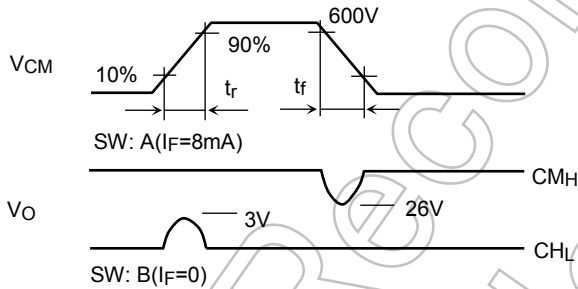
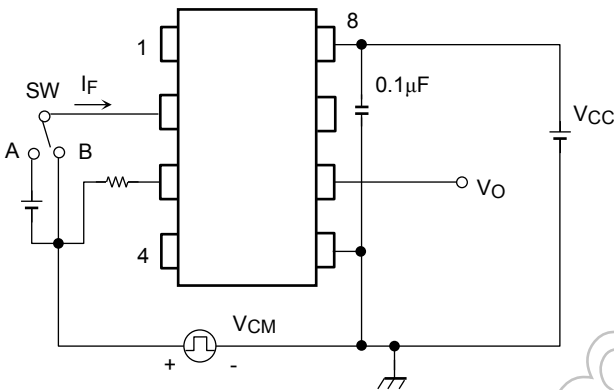
Test Circuit 4 : V_{OL}



Test Circuit 5: t_{pLH} , t_{pHL} , t_r , t_f



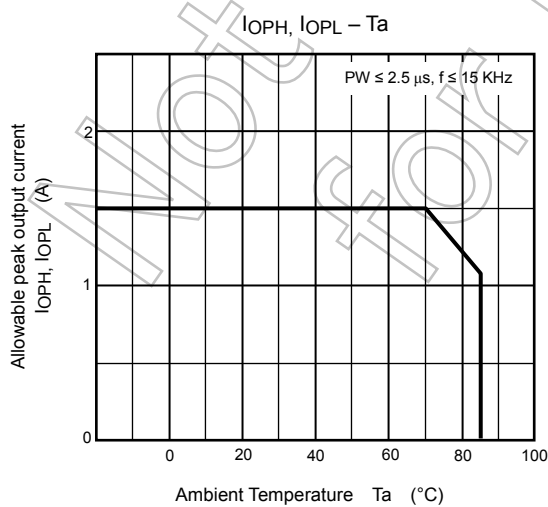
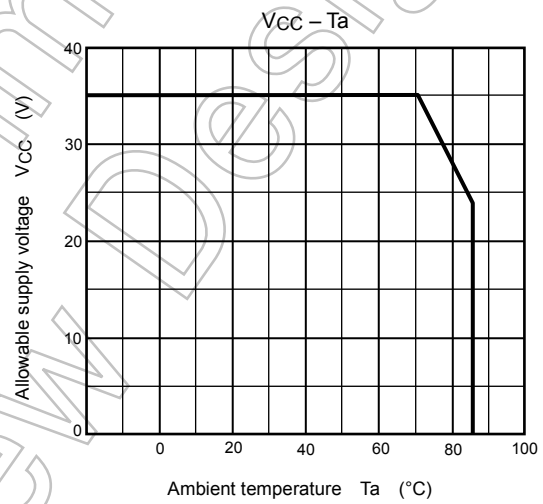
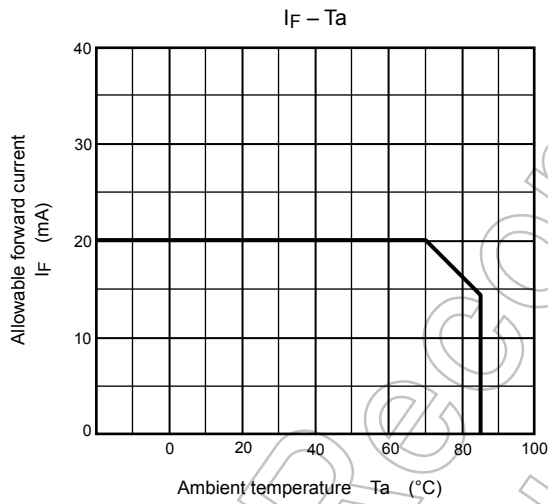
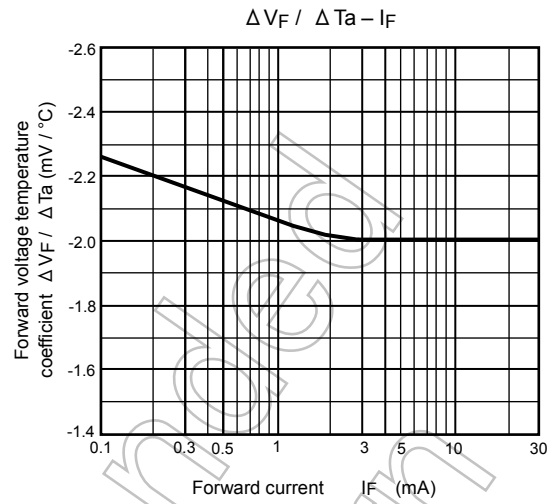
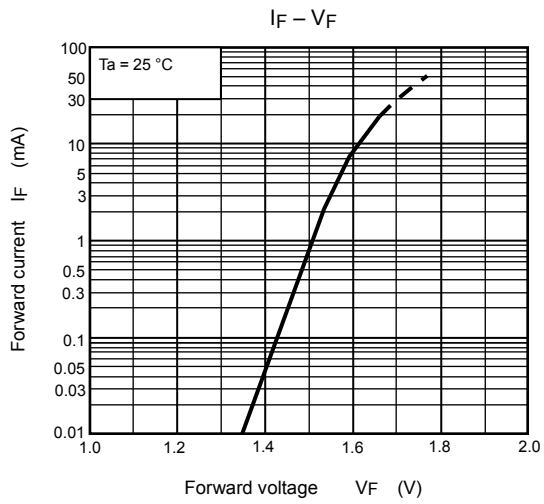
Test Circuit 6: C_{MH} , C_{ML}



$$C_{ML} = \frac{480 \text{ (V)}}{t_r \text{ (}\mu\text{s)}}$$

$$C_{MH} = \frac{480 \text{ (V)}}{t_f \text{ (}\mu\text{s)}}$$

$C_{ML}(C_{MH})$ is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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