



SPLD GAL Family 8 Macro Cells 40MHz 5V 20-Pin PDIP

Manufacturer: <u>Lattice Semiconductor Corp</u>

Package/Case: DIP20

Product Type: Programmable Logic ICs

Lifecycle: Obsolete



Images are for reference only

Inquiry

General Description

The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E2) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Recommended For You

GAL16V8D-25LP GAL16V8D-15QJ GAL16V8D-15LPN

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DIP20 PLCC20 DIP20

GAL16V8D-10LP GAL22V10D-15LJ GAL16V8D-15LJN

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DIP PLCC28 PLCC20

GAL20V8B-15LP GAL16V8D-25LJN GAL16V8D-10LPN

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DIP24 PLCC DIP

GAL16V8D-25QPI

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DIP

GAL22V10D-10LJN

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PLCC

GAL20V8B-15LPN

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DIP

GAL16V8D-25LJI

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PLCC20

GAL18V10B-20LP

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DIP20

GAL16LV8D-5LJ

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