
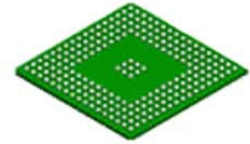


SOC OMAP3 ARM Cortex A8 515-Pin POP-FCBGA Tray

Manufacturer:	Texas Instruments, Inc
Package/Case:	PBGA-515
Product Type:	Embedded Processors & Controllers
RoHS:	RoHS Compliant/Lead free 
Lifecycle:	Active



Images are for reference only

Inquiry

General Description

devices are based on the enhanced OMAP 3 architecture.

The OMAP 3 architecture is designed to provide best-in-class video, image, and graphics processing sufficient to support the following:

- Streaming video
- Video conferencing
- High-resolution still image

The device supports high-level operating systems (HLOSs), such as:

- Linux
- Windows CE
- Android

This OMAP device includes state-of-the-art power-management techniques required for high-performance mobile products.

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor
- PowerVR SGX subsystem for 3D graphics acceleration to support display (OMAP35 device only)
- Camera image signal processor (ISP) that supports multiple formats and interfacing options connected to a wide variety of image sensors
- Display subsystem with a wide variety of features for multiple concurrent image manipulation, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC and PAL video out.
- Level 3 (L3) and level 4 (L4) interconnects that provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals

The device also offers:

A comprehensive power- and clock-management scheme that enables high-performance, low-power operation, and ultralow-power standby features. The device also supports SmartReflex adaptive voltage control. This power-management technique for automatic control of the operating voltage of a module reduces the active power consumption.

Memory-stacking feature using the package-on-package (POP) implementation (CBB and CBC packages only)

OMAP35 devices are available in a 515-pin s-PBGA package (CBB suffix), 515-pin s-PBGA package (CBC suffix), and a 423-pin s-PBGA package (CUS suffix). Some features of the CBB and CBC packages are not available in the CUS package. (See Table 1-1 for package differences).

This data manual presents the electrical and mechanical specifications for the OMAP35 applications processors. The information in this data manual applies to both the commercial and extended temperature versions of the OMAP35 applications processors unless otherwise indicated. This data manual consists of the following sections:

- Section 2: Terminal Description: assignment, electrical characteristics, multiplexing, and functional description
- Section 3: Electrical Characteristics: power domains, operating conditions, power consumption, and DC characteristics
- Section 4: Clock Specifications input and output clocks, DPLL and DLL
- Section 5: Video Dac Specifications
- Section 6: Timing Requirements and Switching Characteristics
- Section 7: Package Characteristics: thermal characteristics, device nomenclature, and mechanical data for available packaging

Key Features

OMAP3 Devices:

MPU Subsystem

NEON SIMD Coprocessor

Tile-Based Architecture Delivering up to 1 MPoly/sec

Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality

Industry Standard API Support: OpenGL ES 1.1 and 2.0, OpenVG1.0

Fine-Grained Task Switching, Load Balancing, and Power Management

Programmable High-Quality Image Anti-Aliasing

Fully Software-Compatible with ARM9

Commercial and Extended Temperature Grades

ARM Cortex-A8 Core

ARMv7 Architecture

TrustZone

Thumb-2

MMU Enhancements

In-Order, Dual-Issue, Superscalar Microprocessor Core

NEON Multimedia Architecture

Over 2x Performance of ARMv6 SIMD

Supports Both Integer and Floating-Point SIMD

Jazelle RCT Execution Environment Architecture

Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer, and 8-Entry Return Stack

Embedded Trace Macrocell (ETM) Support for Noninvasive Debug

ARM Cortex-A8 Memory Architecture:

112KB of ROM

64KB of Shared SRAM

Endianness:

ARM Instructions – Little Endian

ARM Data – Configurable

External Memory Interfaces:

General Purpose Memory Controller (GPMC)

16-Bit-Wide Multiplexed Address and Data Bus

Up to 8 Chip-Select Pins with 128-MB Address Space per Chip-Select Pin

Glueless Interface to NOR Flash, NAND Flash (with ECC Hamming Code Calculation), SRAM, and Pseudo-SRAM

Flexible Asynchronous Protocol Control for Interface to Custom Logic (FPGA, CPLD, ASICs, and so forth)

Nonmultiplexed Address and Data Mode (Limited 2-KB Address Space)

System Direct Memory Access (sDMA) Controller (32 Logical Channels with Configurable Priority)

Camera Image Signal Processor (ISP)

CCD and CMOS Imager Interface

Memory Data Input

BT.601 (8-Bit) and BT.656 (10-Bit) Digital YCbCr 4:2:2 Interface

Glueless Interface to Common Video Decoders

Resize Engine

Resize Images From 1/4x to 4x

Separate Horizontal and Vertical Control

Display Subsystem

Parallel Digital Output

Up to 24-Bit RGB

HD Maximum Resolution

Supports Up to 2 LCD Panels

Support for Remote Frame Buffer Interface (RFBI) LCD Panels

2 10-Bit Digital-to-Analog Converters (DACs) Supporting:

Composite NTSC and PAL Video

Luma and Chroma Separate Video (S-Video)

Rotation 90-, 180-, and 270-Degrees

Resize Images From 1/4x to 8x

Color Space Converter

8-Bit Alpha Blending

Serial Communication

5 Multichannel Buffered Serial Ports (McBSPs)

512-Byte Transmit and Receive Buffer (McBSP1, McBSP3, McBSP4, and McBSP5)

5-KB Transmit and Receive Buffer (McBSP2)

SIDETONE Core Support (McBSP2 and McBSP3 Only) For Filter, Gain, and Mix Operations

Direct Interface to I2S and PCM Device and TDM Buses

128-Channel Transmit and Receive Mode

Four Master or Slave Multichannel Serial Port Interface (McSPI) Ports

High-, Full-, and Low-Speed USB OTG Subsystem (12- and 8-Pin ULPI Interface)

High-, Full-, and Low-Speed Multiport USB Host Subsystem

12- and 8-Pin ULPI Interface or 6-, 4-, and 3-Pin Serial Interface

One HDQ/1-Wire Interface

UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)

Three Master and Slave High-Speed Inter-Integrated Circuit (I2C) Controllers

Removable Media Interfaces:

Three Multimedia Card (MMC)/Secure Digital (SD) with Secure Data I/O (SDIO)

Comprehensive Power, Reset, and Clock Management

SmartReflex Technology

Dynamic Voltage and Frequency Scaling (DVFS)

Test Interfaces

IEEE 1149.1 (JTAG) Boundary-Scan Compatible

ETM Interface

Serial Data Transport Interface (SDTI)

12 32-Bit General-Purpose Timers

2 32-Bit Watchdog Timers

1 32-Bit 32-kHz Sync Timer

Up to General-Purpose I/O (GPIO) Pins (Multiplexed with Other Device Functions)

Package-On-Package (POP) Implementation for Memory Stacking (Not Available in CUS Package)

Discrete Memory Interface

Packages:

1.8-V I/O and 3.0-V (MMC1 Only),

Recommended For You

OMAPL138EZWT3

Texas Instruments, Inc

BGA361

OMAP3530DCUS

Texas Instruments, Inc

BGA

OMAPL138BZWID4

Texas Instruments, Inc

BGA

OMAP3530ECBBA

Texas Instruments, Inc

BGA

OMAPL137BPTPH

Texas Instruments, Inc

MCU

OMAPL138BZWT4

Texas Instruments, Inc

BGA

SMOMAPL138BGWTA3R

Texas Instruments, Inc

BGA

OMAPL138BGWTMEP

Texas Instruments, Inc

BGA

OMAPL138BZWTA3R

Texas Instruments, Inc

361-LFBGA

OMAP5910GGZG2

Texas Instruments, Inc

BGA

OMAPL138BZCE3

Texas Instruments, Inc

NFBGA

OMAP3530DZCBB

Texas Instruments, Inc

FCBGA515

OMAP3503DCBC

Texas Instruments, Inc

515-VFBGAFCBGA

XOMAP3515BCBB

Texas Instruments, Inc

515-VFBGAFCBGA

OMAP3530EZCBB

Texas Instruments, Inc

515-VFBGAFCBGA