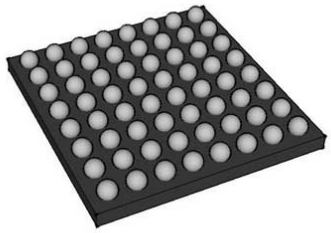
ADSP-TS101SAB1-100

DSP Fixed-Point/Floating-Point 128bit 300MHz 625-Pin BGA Tray



Images are for reference only

Inquiry

Manufacturer:	Analog Devices, Inc
Package/Case:	BGA
Product Type:	Embedded Processors & Controllers
Lifecycle:	Obsolete

General Description

The ADSP-TS101S is the first member of the TigerSHARC Processor family. Targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally-intensive real-time functions, ADI's TigerSHARC processor is well-suited to video and communication markets, including the 3G cellular and broadband wireless base stations, as well as defense, medical imaging, industrial instrumentation. The ADSP-TS101S features a static superscaler architecture which combines RISC, VLIW and standard DSP functionality. Native support of fixed and floating point data types, coupled with the leading edge multiprocessing capabilities allows the TigerSHARC processor to offer unrivaled DSP performance. At a 300 MHz clock rate, the ADSP-TS101S offers the industry's highest 16-bit fixed-point performance and a 32-bit floating 1024-point complex FFT time of 32.5 microseconds.

ADSP-TS101S Performance:
High performance 300 MHz, 3.3 ns instruction rate DSP core
Executes eight 16-bit MACs with 40-bit accumulation or two 32-bit MACs with 80-bit accumulation per cycle
Executes six single-precision floating point or twenty four 16-bit fixed point operations per cycle (1800 MFLOPS or 7.2 GOPS performance)
8-cycle instruction pipeline; 3-cycle fetch pipe and 5-cycle execution pipe
Parallelism allows the execution of up to four 32-bit instructions per cycle
The ADSP-TS101S is available in both 19mm X 19mm and 27mm X 27mm inexpensive, plastic ball-grid array packages. The TigerSHARC is available for general purpose sampling today.

Key Features

Static Superscalar architecture which supports 1, 8, 16 and 32-bit fixed point as well as floating point data processing

High performance 300 MHz, 3.3 ns instruction rate DSP core

6 Mbit on-chip SRAM internally organized in three banks with user-defined partitioning

14 channel, zero overhead DMA controller

Enhanced communications instruction set for wireless infrastructure applications allows for the TigerSHARC to offer complete base band processing

Three internal 128-bit wide internal buses providing a total memory bandwidth of 14.4 Gbytes per second

Software radio approach allows for the adoption of a single platform for multiple wireless telecommunication standards

Single instruction multiple-data (SIMD) operation supported by two computation blocks each with an ALU, multiplier, shifter and 32-word register file

Assembly and C language programmability

Recommended For You

ADSP-BF592KCPZ
Analog Devices, Inc
LFCSP64

ADSP-2183KSTZ-210
Analog Devices, Inc
QFP100

ADSP-BF534BBCZ-4B
Analog Devices, Inc
BGA

ADSP-BF537BBCZ-5A
Analog Devices, Inc
CSPBGA-182

ADSP-BF532SBSTZ400
Analog Devices, Inc
LQFP176

ADSP-BF533SBBCZ500
Analog Devices, Inc
BGA

ADSP-BF533SKBCZ-6V
Analog Devices, Inc
BGA

ADSP-BF533SBBZ500
Analog Devices, Inc
BGA

ADSP-BF533SBSTZ400
Analog Devices, Inc
QFP

ADSP-BF533SBBCZ400
Analog Devices, Inc
BGA160

ADSP-2171BSTZ-133
Analog Devices, Inc
QFP

ADSP-2186MKST-300
Analog Devices, Inc
QFP

ADSP-BF512BSWZ-4
Analog Devices, Inc
QFP176

AD1940YST
Analog Devices, Inc
QFP48

ADSP-BF534BBCZ-5B
Analog Devices, Inc
BGA