LAN9218-MT

Ethernet CTLR Single Chip 10Mbps/100Mbps 3.3V 100-Pin TQFP Tray

Manufacturer:	Microchip Technology, Inc
Package/Case:	TQFP100
Product Type:	Communication & Networking ICs
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The LAN9218(i) is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9218(i) has been specifically architected to provide the highest performance possible for any given architecture. The LAN9218(i) is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

The LAN9218(i) includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit and 32-bit microprocessors and microcontrollers. The LAN9218(i) includes large transmit and receive data FIFOs with a high-speed host bus interface to accommodate high bandwidth, high latency applications. In addition, the LAN9218(i) memory buffer architecture allows the most efficient use of memory resources by optimizing packet granularity.

The 93AA46AE48 EEPROM device from Microchip comes with a factory programmed, globally unique EUI-48™ MAC Address. This Ethernet controller will automatically detect and load the EUI-48™ node address from the 93AA46AE48 EEPROM at start-up or reset. *The LANCheck online design review service is subject to Microchip's Program Terms and Conditions and requires a myMicrochip account.

Key Features

Optimized for the highest performance applications

Efficient architecture with low CPU overhead

Easily interfaces to most 32-bit and 16-bit embedded CPU's

Integrated PHY with HP Auto-MDIX support

Highest performing non-PCI Ethernet controller

32-bit interface with fast bus cycle times

Burst-mode read support

Internal buffer memory can store over 200 packets

Automatic PAUSE and back-pressure flow control

Supports Slave-DMA

Interrupt pin with programmable hold-off timer

Reduces system cost and increases design flexibility

SRAM-like interface easily interfaces to most embedded CPU's or SoC's

Fully compliant with IEEE 802.3/802.3u standards

Integrated Ethernet MAC and PHY

Full- and half-duplex support

Full-duplex flow control

Backpressure for half-duplex flow control

Preamble generation and removal

Automatic 32-bit CRC generation and checking

Recommended For You

LAN91C111-NE

Microchip Technology, Inc

QFP

LAN91C93I-MU

Microchip Technology, Inc

QFP

LAN9420I-NU

Microchip Technology, Inc

TQFP128

LAN91C96-MU

Microchip Technology, Inc

TQFP100

LAN91C111i-NC

Microchip Technology, Inc

QFP

LAN91C96-MS

Microchip Technology, Inc

QFP

LAN91C111I-NU

Microchip Technology, Inc

TQFP128

LAN91C111-NC

Microchip Technology, Inc

QFP

LAN9252I/ML

Microchip Technology, Inc

QFN-64

LAN9215-MT

Microchip Technology, Inc

QFP100

LAN91C111I-NS

Microchip Technology, Inc

QFP128

LAN91C111-NU

Microchip Technology, Inc

QFP

LAN9118-MT

Microchip Technology, Inc

TQFP100

LAN9252I/PT

Microchip Technology, Inc

TQFP64

LAN9221I-ABZJ

Microchip Technology, Inc

QFN56