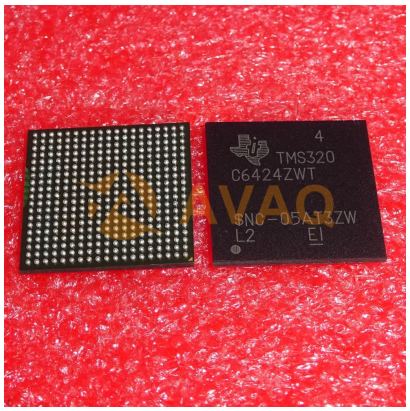
TMS320C6424ZWT4

DSP Fixed-Point 32bit 400MHz 3200MIPS 361-Pin NFBGA Tray

Manufacturer:	Texas Instruments, Inc
Package/Case:	BGA
Product Type:	Embedded Processors & Controllers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active



Images are for reference only

Inquiry

General Description

The TMS320C64x+ DSPs (including the TMS320C6424 device) are the highest-performance fixed-point DSP generation in the TMS320C6000 DSP platform. The C6424 device is based on the third-generation high-performance, advanced VelociTI very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for digital signal processor applications. The C64x+ devices are upward code-compatible from previous devices that are part of the C6000 DSP platform. The C64x DSPs support added functionality and have an expanded instruction set from previous devices.

Any reference to the C64x DSP or C64x CPU also applies, unless otherwise noted, to the C64x+ DSP and C64x+ CPU, respectively.

With performance of up to 4800 million instructions per second (MIPS) at a clock rate of 600 MHz, the C64x+ core offers solutions to high-performance DSP programming challenges. The DSP core possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. The C64x+ DSP core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units-two multipliers for a 32-bit result and six arithmetic logic units (ALUs). The eight functional units include instructions to accelerate the performance in telecom, audio, and industrial applications. The DSP core can produce four 16-bit multiply-accumulates (MACs) per cycle for a total of 2400 million MACs per second (MMACS), or eight 8-bit MACs per cycle for a total of 4800 MMACS. For more details on the C64x+ DSP, see the TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide (literature number SPRU732).

The C6424 also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals similar to the other C6000 DSP platform devices. The C6424 core uses a two-level cache-based architecture. The Level 1 program memory/cache (L1P) consists of a 256K-bit memory space that can be configured as mapped memory or direct mapped cache, and the Level 1 data (L1D) consists of a 640K-bit memory space–384K-bit of which is mapped memory and 256K-bit of which can be configured as mapped memory or 2-way set-associative cache. The Level 2 memory/cache (L2) consists of a 1M-bit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two.

The peripheral set includes: a 10/100 Mb/s Ethernet MAC (EMAC) with a management data input/output (MDIO) module; a 4-bit transmit, 4-bit receive VLYNQ interface; an inter-integrated circuit (I2C) Bus interface; two multichannel buffered serial ports (McBSPs); a multichannel audio serial port (McASP0) with 4 serializers; 2 64-bit general-purpose timers each configurable as 2 independent 32-bit timers; 1 64-bit watchdog timer; a user-configurable 16-bit host-port interface (HPI); up to 111-pins of general-purposeinput/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; 2 UARTs with hardware handshaking support on 1 UART; 3 pulse width modulator (PWM) peripherals; 1 peripheral component interconnect (PCI) [33 MHz]; and 2 glueless external memory interfaces: an asynchronous external memory interface (EMIFA) for slower memories/peripherals, and a higher speed synchronous memory interface for DDR2.

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the C6424 and the network. The C6424 EMAC supports 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The I2C and VLYNQ ports allow C6424 to easily control peripheral devices and/or communicate with host processors.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections later in this document and the associated peripheral reference guides.
The C6424 has a complete set of development tools. These include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source code execution.

Key Features

High-Performance Digital Signal Processor (C6424)

2.5-, 2-, 1.67, 1.43-ns Instruction Cycle Time

400-, 500-, 600-MHz C64x+ Clock Rate

Eight 32-Bit C64x+ Instructions/Cycle

3200, 4000, 4800, 5600 MIPS

Fully Software-Compatible With C64x

Commercial and Automotive (Q or S suffix)Grades

Low-Power Device (L suffix)

VelociTI.2 Extensions to VelociTI Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+ DSP Core

Eight Highly Independent Functional Units With VelociTI.2 Extensions:

Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle

Two Multipliers Support Four 16 × 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 × 8-Bit Multiplies (16-Bit Results) per Clock Cycle

Load-Store Architecture With Non-Aligned Support

64 32-Bit General-Purpose Registers

Instruction Packing Reduces Code Size

All Instructions Conditional

Additional C64x+ Enhancements

Protected Mode Operation

Exceptions Support for Error Detection and Program Redirection

Hardware Support for Modulo Loop Auto-Focus Module Operation

C64x+ Instruction Set Features

Byte-Addressable (8-/16-/32-/64-Bit Data)

8-Bit Overflow Protection

Bit-Field Extract, Set, Clear

Normalization, Saturation, Bit-Counting

VelociTI.2 Increased Orthogonality

C64x+ Extensions

Compact 16-bit Instructions

Additional Instructions to Support Complex Multiplies

C64x+ L1/L2 Memory Architecture

256K-Bit (32K-Byte) L1P Program RAM/Cache [Flexible Allocation]

640K-Bit (80K-Byte) L1D Data RAM/Cache [Flexible Allocation]

1M-Bit (128K-Byte) L2 Unified Mapped RAM/Cache [Flexible Allocation]

Endianess: Supports Both Little Endian and Big Endian

External Memory Interfaces (EMIFs)

32-Bit DDR2 SDRAM Memory Controller With 256M-Byte Address Space (1.8-V I/O)

Supports up to 333-MHz (data rate) bus and interfaces to DDR2-400 SDRAM

Asynchronous 16-Bit Wide EMIF (EMIFA) With up to 128M-Byte Address Reach

Flash Memory Interfaces

NOR (8-/16-Bit-Wide Data)

NAND (8-/16-Bit-Wide Data)

Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)

Two 64-Bit General-Purpose Timers (Each Configurable as Two 32-Bit Timers)

One 64-Bit Watch Dog Timer

Two UARTs (One with RTS and CTS Flow Control)

Master/Slave Inter-Integrated Circuit (I2C Bus)

Two Multichannel Buffered Serial Ports (McBSPs)

I2S and TDM

AC97 Audio Codec Interface

SPI

Standard Voice Codec Interface (AIC12)

Telecom Interfaces - ST-Bus, H-100

128 Channel Mode

Multichannel Audio Serial Port (McASP0)

Four Serializers and SPDIF (DIT) Mode

16-Bit Host-Port Interface (HPI)

32-Bit 33-MHz, 3.3-V Peripheral Component Interconnect (PCI) Master/Slave Interface

10/100 Mb/s Ethernet MAC (EMAC)

IEEE 802.3 Compliant

Supports Multiple Media Independent Interfaces (MII, RMII)

Management Data Input/Output (MDIO) Module

VLYNQ Interface (FPGA Interface)

Three Pulse Width Modulator (PWM) Outputs

On-Chip ROM Bootloader

Individual Power-Savings Modes

Flexible PLL Clock Generators

IEEE-1149.1 (JTAG) Boundary-Scan-Compatible

Up to 111 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)

Packages:

361-Pin Pb-Free PBGA Package (ZWT Suffix), 0.8-mm Ball Pitch

376-Pin Plastic BGA Package (ZDU Suffix), 1.0-mm Ball Pitch

0.09-µm/6-Level Cu Metal Process (CMOS)

3.3-V and 1.8-V I/O, 1.2-V Internal (-7/-6/-5/-4/-Q6/-Q5/-Q4)

3.3-V and 1.8-V I/O, 1.05-V Internal (-7/-6/-5/-4/-L/-Q5)

APPLICATIONS

Telecom

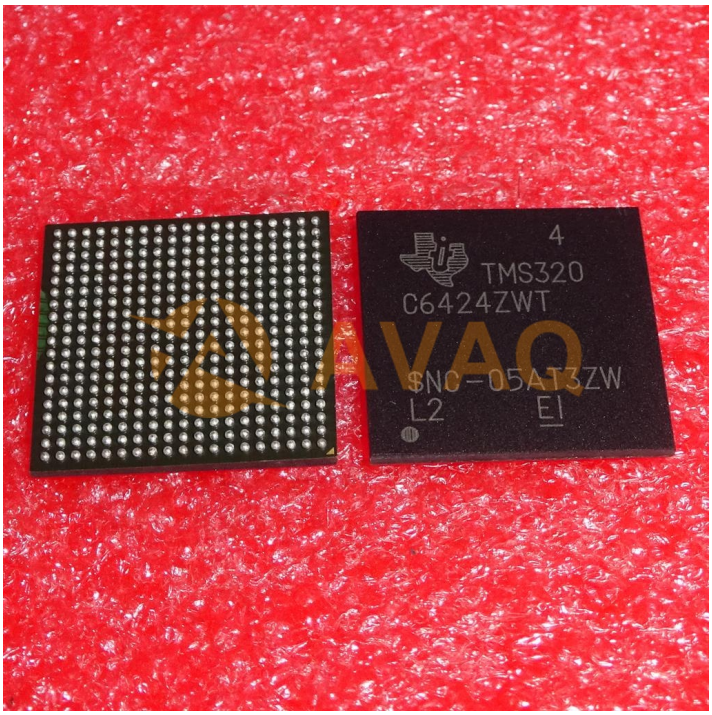
Audio

Industrial Applications

Community Reesources

TI E2E Community

TI Embedded Processors Wiki



Recommended For You

TMS320DM642AZNZ6

Texas Instruments, Inc

BGA

TMS320C31PQA40

Texas Instruments, Inc

QFP

TMS320C6726BRFP266

Texas Instruments, Inc

QFP144

TMS320DM648ZUTD9

Texas Instruments, Inc

BGA

TMS320C203PZ80

Texas Instruments, Inc

QFP

TMS320F28027PTT

Texas Instruments, Inc

LQFP48

TMS5703137DZWTQQ1

Texas Instruments, Inc

NFBGA-337

TMS34010FNL-40

Texas Instruments, Inc

PLCC

TMS320C6670ACYPA2

Texas Instruments, Inc

FCBGA84

TMS320VC5402APGE16

Texas Instruments, Inc

LQFP-144

TMS320DM642AGDKA5

Texas Instruments, Inc

FCCSP(GDK)

TMS320C6711DZDP250

Texas Instruments, Inc

BGA

TMS320DM365ZCE30

Texas Instruments, Inc

BGA

TMS320DM642AZNZA6

Texas Instruments, Inc

BGA

TMS320C50PQ57

Texas Instruments, Inc

QFP132