

Counter/Divider Single 5-Bit Decade UP 16-Pin PDIP Tube

Manufacturer: <u>Texas Instruments, Inc</u>

Package/Case: DIP

Product Type: Logic ICs

RoHS: RoHS Compliant/Lead free

Lifecycle: Active



Images are for reference only

Inquiry

General Description

CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and /or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (Cout) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Key Features

Counter and 7-segment decoding in one package

Easily interfaced with 7-segment display types

Fully static counter operation: DC to 6 MHz (typ.) at VDD = 10 V

Ideal for low-power displays

Display enable output (CD4026B)

"Ripple blanking" and lamp test (CD4033B)

100% tested for quiescent current at 20 V

Standardized, symmetrical output characteristics

5-V, 10-V, and 15-V parametric ratings

Schmitt-triggered clock inputs

Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

Decade counting 7-segment decimal display

Frequency division 7-segment decimal displays

Clocks, watches, timers (e.g. ÷60, ÷60, ÷12 counter/display)

Counter/display driver for meter applications

Description

CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and /or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs.

Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (Cout) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



Recommended For You

CD4017BE

Texas Instruments, Inc

DIP16

CD74AC161M

Texas Instruments, Inc

SOP16

CD4040BE

Texas Instruments, Inc

DIP16

CD4020BE

Texas Instruments, Inc

DIP16

CD4510BNSR

Texas Instruments, Inc

SOP16

CD40193BE

Texas Instruments, Inc

DIP

CD4060BM

Texas Instruments, Inc

SOP

CD4516BE

Texas Instruments, Inc

DIP16

CD40110BE

Texas Instruments, Inc

DIP

CD4022BE

Texas Instruments, Inc

DIP

CD4024BM

Texas Instruments, Inc

SOP14

CD4520BE

Texas Instruments, Inc

DIP16

CD4060BE

Texas Instruments, Inc

DIP16

CD74HCT193E

Texas Instruments, Inc

DIP

CD74HC193E

Texas Instruments, Inc

DIP