TMS320C6711DZDP250

DSP Floating-Point 32bit 250MHz 2000MIPS 272-Pin BGA Tray

Manufacturer:	Texas Instruments, Inc
Package/Case:	BGA
Product Type:	Embedded Processors & Controllers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The TMS320C67x DSPs (including the TMS320C6711, TMS320C6711B, TMS320C6711C, TMS320C6711D devices) compose the floating-point DSP family in the TMS320C6000 DSP platform. The C6711, C6711B, C6711C, and C6711D devices are based on the high-performance, advanced very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for multichannel and multifunction applications.

With performance of up to 1200 million floating-point operations per second (MFLOPS) at a clock rate of 200 MHz or up to 1500 MFLOPS at a clock rate of 250 MHz, the C6711D device also offers cost-effective solutions to high-performance DSP programming challenges. The C6711D DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide four floating-/fixed-point ALUs, two fixed-point ALUs, and two floating-/fixed-point multipliers. The C6711D can produce two MACs per cycle for a total of 400 MMACS.

The C6711D DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

The C6711D device uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 32-Kbit direct mapped cache and the Level 1 data cache (L1D) is a 32-Kbit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of a 512-Kbit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM, SBSRAM and asynchronous peripherals.

The C6711D has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source code execution.

Key Features

Excellent-Price/Performance Floating-Point Digital Signal Processor (DSP):

TMS320C6711D

Eight 32-Bit Instructions/Cycle

167-, 200-, 250-MHz Clock Rates

6-, 5-, 4-ns Instruction Cycle Time

1000, 1200, 1500 MFLOPS

Advanced Very Long Instruction Word (VLIW) C67x DSP Core

Eight Highly Independent Functional Units:

Four ALUs (Floating- and Fixed-Point)

Two ALUs (Fixed-Point)

Two Multipliers (Floating- and Fixed-Point)

Load-Store Architecture With 32 32-Bit General-Purpose Registers

Instruction Packing Reduces Code Size

All Instructions Conditional

Instruction Set Features

Hardware Support for IEEE Single-Precision and Double-Precision Instructions

Byte-Addressable (8-, 16-, 32-Bit Data)

8-Bit Overflow Protection

Saturation

Bit-Field Extract, Set, Clear

Bit-Counting

Normalization

L1/L2 Memory Architecture

32K-Bit (4K-Byte) L1P Program Cache (Direct Mapped)

32K-Bit (4K-Byte) L1D Data Cache (2-Way Set-Associative)

512K-Bit (64K-Byte) L2 Unified Mapped RAM/Cache (Flexible Data/Program Allocation)

Device Configuration

Boot Mode: HPI, 8-, 16-, 32-Bit ROM Boot

Endianness: Little Endian, Big Endian

Enhanced Direct-Memory-Access (EDMA) Controller (16 Independent Channels)

32-Bit External Memory Interface (EMIF)

Glueless Interface to Asynchronous Memories: SRAM and EPROM

Glueless Interface to Synchronous Memories: SDRAM and SBSRAM

256M-Byte Total Addressable External Memory Space

16-Bit Host-Port Interface (HPI)

Two Multichannel Buffered Serial Ports (McBSPs)

Direct Interface to T1/E1, MVIP, SCSA Framers

ST-Bus-Switching Compatible

Up to 256 Channels Each

AC97-Compatible

Serial-Peripheral-Interface (SPI) Compatible (Motorola)

Two 32-Bit General-Purpose Timers

Flexible Software Configurable PLL-Based Clock Generator Module

A Dedicated General-Purpose Input/Output (GPIO) Module With 5 Pins

IEEE-1149.1 (JTAG) Boundary-Scan-Compatible

272-Pin Ball Grid Array (BGA) Package (GDP and ZDP Suffixes)

CMOS Technology

0.13-µm/6-Level Copper Metal Process

3.3-V I/O, 1.4-V Internal (-250)

3.3-V I/O, 1.20-V Internal

Recommended For You

TMS320DM642AZNZ6

Texas Instruments, Inc

BGA

TMS320C31PQA40

Texas Instruments, Inc

QFP

TMS320C6726BRFP266

Texas Instruments, Inc

QFP144

TMS320DM648ZUTD9

Texas Instruments, Inc

BGA

TMS320C203PZ80

Texas Instruments, Inc

QFP

TMS320F28027PTT

Texas Instruments, Inc

LQFP48

TMS5703137DZWTQQ1

Texas Instruments, Inc

NFBGA-337

TMS34010FNL-40

Texas Instruments, Inc

PLCC

TMS320C6670ACYPA2

Texas Instruments, Inc

FCBGA84

TMS320VC5402APGE16

Texas Instruments, Inc

LQFP-144

TMS320DM642AGDKA5

Texas Instruments, Inc

FCCSP(GDK)

TMS320C6424ZWT4

Texas Instruments, Inc

BGA

TMS320DM365ZCE30

Texas Instruments, Inc

BGA

TMS320DM642AZNZA6

Texas Instruments, Inc

BGA

TMS320C50PQ57

Texas Instruments, Inc

QFP132