

DPAK (SINGLE GAUGE) CASE 369C ISSUF F

DATE 21 JUL 2015

NOTES:

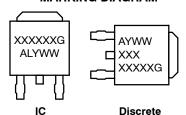
- NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: INCHES. 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-

- MENSIONS b3, L3 and Z.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
 5. DIMENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY.

 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE.

		INCHES		MILLIMETERS	
Į	DIM	MIN	MAX	MIN	MAX
	Α	0.086	0.094	2.18	2.38
	A 1	0.000	0.005	0.00	0.13
	b	0.025	0.035	0.63	0.89
	b2	0.028	0.045	0.72	1.14
	b3	0.180	0.215	4.57	5.46
	С	0.018	0.024	0.46	0.61
	c2	0.018	0.024	0.46	0.61
	D	0.235	0.245	5.97	6.22
ſ	Е	0.250	0.265	6.35	6.73
	е	0.090 BSC		2.29 BSC	
	Н	0.370	0.410	9.40	10.41
	L	0.055	0.070	1.40	1.78
	L1	0.114 REF		2.90 REF	
l	L2	0.020	BSC	0.51 BSC	
	L3	0.035	0.050	0.89	1.27
[L4		0.040		1.01
[Z	0.155		3.93	

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code = Assembly Location Α

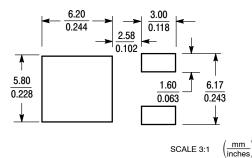
L = Wafer Lot Υ = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "=", may or may not be present. Some products may not follow the Generic Marking.

1 2 7	100	1330E F		
3 SCALE 1:1				
L3 — B B D NOTE 7	DETAIL A H C SIDE VIEW	BOTTOM VIEW		
TOP VIEW 0.005 (0	0.13) (M) C	<u></u>		
L2 GAUGE PLANE	C SEATING PLANE	Z ↑		
$ \uparrow \qquad \leftarrow L \rightarrow \qquad \qquad A1^{\uparrow} $		M VIEW		
DETAIL A ROTATED 90 CW		UCTIONS		

STYLE 1: PIN 1. BASE 2. COLLEC 3. EMITTEF 4. COLLEC	R 3. SOUI	N 2. CAT RCE 3. ANC	HODE 2. ANODE DDE 3. GATE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUS 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE T 3. CATHODE 4. ANODE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1	

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