AVAQ

MCU 16-bit MSP430 RISC 15.5KB Flash 2.5V/3.3V 64-Pin LQFP T/R

Manufacturer:	Texas Instruments, Inc
Package/Case:	LQFP64
Product Type:	Embedded Processors & Controllers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active

Images are for reference only

Inquiry

General Description

The SN74AUP1T34-Q1 device is a 1-bit noninverting translator that uses two separate configurable power-supply rails. It is a unidirectional translator from A to B. The A port is designed to track V_{CCA}. V_{CCA} accepts supply voltages from 0.9 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts supply voltages from 0.9 V to 3.6 V. This allows for low-voltage translation between 1-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes. The SN74AUP1T34-Q1 is also fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The VCC isolation feature ensures that if V_{CCA} input is at GND, the B port is in the high-impedance state. If V_{CCB} input is at GND, any input to the A side does not cause the leakage current even floating.

Key Features

Qualified for Automotive Applications

AEC-Q100 Qualified

Device Temperature Grade 1: –40°C to 125°C

Ambient Operating Temperature

Device HBM ESD Classification Level 3A

Device CDM ESD Classification Level C5

Wide Operating VCC Range of 0.9 V to 3.6 V

Balanced Propagation Delays: t

PLH

PHL

Low Static-Power Consumption: Maximum of 5-µA

ICC

I

off

VCC Isolation Feature – If V

CCA

B Port Is in the High-Impedance state

Input Hysteresis Allows Slow Input Transition and

Better Switching Noise Immunity at Input

ESD Protection Exceeds JESD 22

5000-V Human-Body Model (AEC-Q100-002-E)

Latch-Up Performance Meets

100 mA Per Q100-004-D
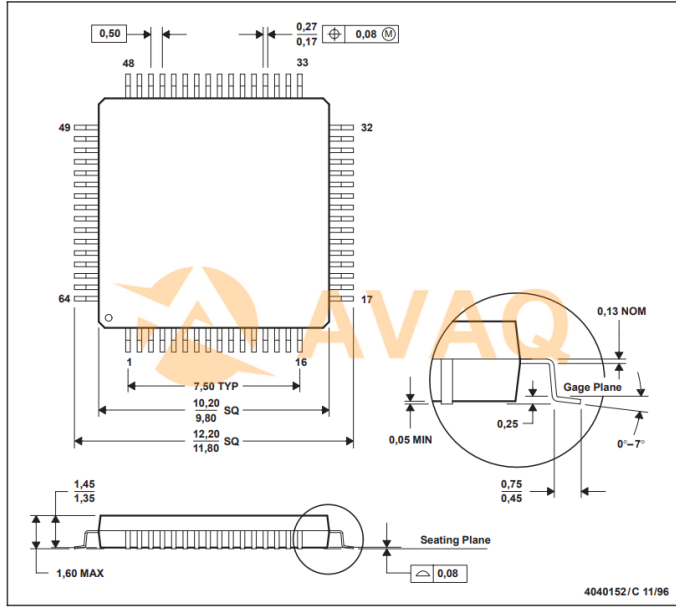
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026.
D. May also be thermally enhanced plastic with leads connected to the die pads.

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1.4 Functional Block Diagram
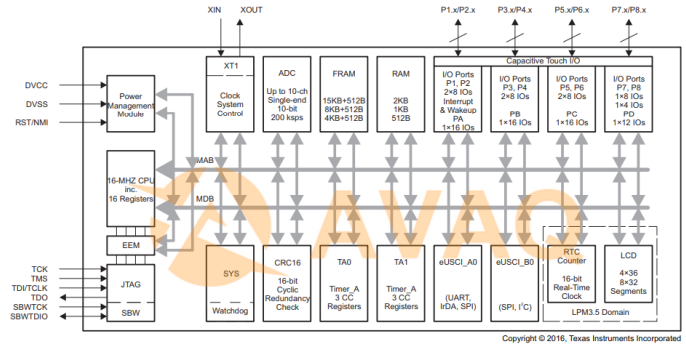
Figure 1-1 shows the functional block diagram.

Figure 1-1. Functional Block Diagram

- The device has one main power pair of DVCC and DVSS that supplies both digital and analog modules. Recommended bypass and decouple capacitors are 4.7 µF to 10 µF and 0.1 µF, respectively, with ±5% accuracy.
- P1 and P2 feature the pin-interrupt function and can wake the MCU from LPM3.5.
- Each Timer_A3 has three CC registers, but only the CCR1 and CCR2 are externally connected. CCR0 registers can only be used for internal period timing and interrupt generation.
- In LPM3.5, the RTC counter and the LCD can be functional while the rest of peripherals are off.
- All I/Os can be configured as Capacitive Touch I/Os.

Recommended For You

TMS320DM642AZNZ6	**TMS320C31PQA40**	**TMS320C6726BRFP266**
Texas Instruments, Inc	Texas Instruments, Inc	Texas Instruments, Inc
BGA	QFP	QFP144
MSP430F147IPM	**MSP430F135IPMR**	**TMS320DM648ZUTD9**
Texas Instruments, Inc	Texas Instruments, Inc	Texas Instruments, Inc
QFP64	LQFP64	BGA
TMS320C203PZ80	**MSP430G2452IPW20**	**MSP430G2231IPW14R**
Texas Instruments, Inc	Texas Instruments, Inc	Texas Instruments, Inc
QFP	TSSOP20	TSSOP14
TMS320F28027PTT	**TMS5703137DZWTQQ1**	**TMS34010FNL-40**
Texas Instruments, Inc	Texas Instruments, Inc	Texas Instruments, Inc
LQFP48	NFBGA-337	PLCC
TMS320C6670ACYPA2	**TMS320VC5402APGE16**	**TMS320DM642AGDKA5**
Texas Instruments, Inc	Texas Instruments, Inc	Texas Instruments, Inc
FCBGA84	LQFP-144	FCCSP(GDK)