AVAQ

## Conv DC-DC 2.2V to 7V Step Up Single-Out 21V 5-Pin SOT-23 T/R

| Manufacturer: | Texas Instruments, Inc |
| :--- | :--- |
| Package/Case: | SOT23-5 |
| Product Type: | Power Management ICs |
| RoHS: | RoHS Compliant/Lead free Rools |

## Lifecycle:

## Active



Images are for reference only

## General Description

The TPS65917-Q1 PMIC integrates five configurable step-down converters with up to 3.5 A of output current to power the processor core, memory, I/O, and preregulation of LDOs The device is AEC-Q100 qualified. The step-down converters are synchronized to an internal 2.2-MHz clock to improve EMC performance of the device. The GPIO_3 pin allows the step-down converters to synchronize to an external clock, allowing multiple devices to synchronize to the same clock which improves system-level EMC performance. The device also contains five LDOs to power low-current or low-noise domains.
The power-sequence controller uses one-time programmable (OTP) memory to control the power sequences, as well as default configurations such as output voltage and GPIO configurations. The OTP is factory-programmed to allow start-up without any software required. Most static settings can be changed from the default through SPI or $\mathrm{I}^{2} \mathrm{C}$ to configure the device to meet many different system needs. For example, voltage-scaling registers are used to support dynamic voltage-scaling requirements of processors.As an additional safety feature, the he OTP also contains a bit-integrity-error detection feature to stop the power-up sequence if an error is detected, preventing the system from starting in an unknown state.
The TPS65917-Q1 device also includes an analog-to-digital converter (ADC) to monitor the system state. The GPADC includes two external channels to monitor any external voltage, as well as internal channels to measure supply voltage, output current, and die temperature, allowing the processor to monitor the health of the system. The device offers a watchdog to monitor for software lockup, and includes protection and diagnostic mechanisms such as short-circuit protection, thermal monitoring, shutdown, and automatic ADC conversions to detect if a voltage is below a predefined threshold. The PMIC can notify the processor of these events through the interrupt handler, allowing the processor to take action in response.

## Key Features

Qualified for Automotive Applications
AEC-Q100 Qualified With the Following Results:
Device Temperature Grade 2: $-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ Ambient Operating Temperature Range
Device HBM Classification Level 2
Device CDM Classification Level C4B
System Voltage Range from 3.135 V to 5.25 V
Low-Power Consumption
$20 \mu \mathrm{~A}$ in Off Mode
$90 \mu \mathrm{~A}$ in Sleep Mode With Two SMPSs Active
0.7 - to $3.3-$ V Output Range in 10 - or $20-\mathrm{mV}$ Steps

Two SMPS Regulators With 3.5-A Capability, With the Ability to Combine into 7-A Output in Dual-Phase Configuration, With Differential Remote Sensing (Output and Ground)

Three Other SMPS Regulators with 3-A, 2-A, and 1.5-A Capabilities

Dynamic Voltage Scaling (DVS) Control and Output Current Measurement in 3.5-A and 3-A SMPS Regulators

Hardware and Software Controlled Eco-mode Supplying up to 5 mA

Short-Circuit Protection

Power-Good Indication (Voltage and Overcurrent Indication)

Internal Soft-Start for In-Rush Current Limitation

Ability to Synchronize to External Clock between 1.7 MHz and 2.7 MHz

Five Low-Dropout (LDO) Linear Regulators:
0 .9- to $3.3-\mathrm{V}$ Output Range in $50-\mathrm{mV}$ steps
Two With 300-mA Capability and Bypass Mode

One With $100-\mathrm{mA}$ Capability and Capable of Low-Noise Performance up to 50 mA
Two Other LDOs With 200-mA Current Capability

Short-Circuit Protection

12-Bit Sigma-Delta General-Purpose ADC (GPADC) With 8 Input Channels (2 external)

Thermal Monitoring With High Temperature Warning and Thermal Shutdown

Power Sequence Control:
Configurable Power-Up and Power-Down Sequences (OTP)

Configurable Sequences Between the SLEEP and ACTIVE State Transition (OTP)

Three Digital Output Signals that can be Included in the Startup Sequence

Selectable Control Interface:
One SPI for Resource Configurations and DVS Control

Two $\mathrm{I}^{2} \mathrm{C}$ Interfaces.
One Dedicated for DVS Control

One General Purpose $\mathrm{I}^{2} \mathrm{C}$ Interface for Resource Configuration and DVS Control

OTP Bit-Integrity Error Detection With Options to Proceed or Hold Power-Up Sequence and RESET_OUT Release

Package Option:
$7-\mathrm{mm} \times 7-\mathrm{mm} 48$-pin VQFN With $0.5-\mathrm{mm}$ Pitch

## Recommended For You

## LM2438T

Texas Instruments, Inc
TO-220-9

## LMB409HVMY/NOPB

Texas Instruments, Inc
MSOP10

LMB429Q1MHX/NOPB
Texas Instruments, Inc
HTSSOP14

LMB409MY/NOPB
Texas Instruments, Inc MSOP10

LMB409MYX/NOPB

Texas Instruments, Inc
MSOP10

## LM2415T

Texas Instruments, Inc
ZIP11

## LM2467TA

Texas Instruments, Inc

TO-220-9

## LMB509SD/NOPB

Texas Instruments, Inc QFN

LMB405AXMY/NOPB
Texas Instruments, Inc
HVSSOP8

LM2469TA
Texas Instruments, Inc
TO-220-9

LM2407T
Texas Instruments, Inc

ZIP11

## LM3406HVMHX/NOPB

Texas Instruments, Inc

TSSOP14

LM2406T

Texas Instruments, Inc
ZIP11

LM2468TA
Texas Instruments, Inc
TO-220

LMB410XMF/NOPB
Texas Instruments, Inc

SOT23-5

