# TMS320DM642AZNZ6

**DSP Fixed-Point 32bit 600MHz 4800MIPS Automotive 548-Pin FCBGA Tray**

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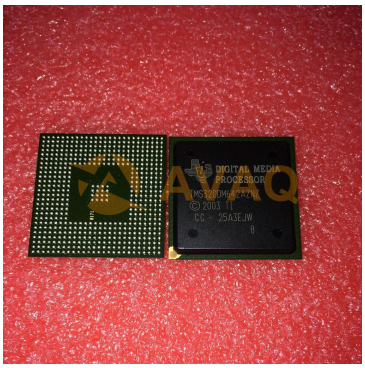
| **Manufacturer:** | Texas Instruments, Inc |
| **Package/Case:** | BGA |
| **Product Type:** | Embedded Processors & Controllers |
| **Lifecycle:** | Active |



Images are for reference only

Inquiry

## General Description

The TMS320C64x DSPs (including the TMS320DM642 device) are the highest-performance fixed-point DSP generation in the TMS320C6000 DSP platform. The TMS320DM642 (DM642) device is based on the second-generation high-performance, advanced VelociTI very-long-instruction-word (VLIW) architecture (VelociTI.2) developed by Texas Instruments (TI), making these DSPs an excellent choice for digital media applications. The C64x is a code-compatible member of the C6000 DSP platform.

With performance of up to 5760 million instructions per second (MIPS) at a clock rate of 720 MHz, the DM642 device offers cost-effective solutions to high-performance DSP programming challenges. The DM642 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. The C64x DSP core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units-two multipliers for a 32-bit result and six arithmetic logic units (ALUs)- with VelociTI.2 extensions. The VelociTI.2 extensions in the eight functional units include new instructions to accelerate the performance in video and imaging applications and extend the parallelism of the VelociTI architecture. The DM642 can produce four 16-bit multiply-accumulates (MACs) per cycle for a total of 2880 million MACs per second (MMACS), or eight 8-bit MACs per cycle for a total of 5760 MMACS. The DM642 DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals similar to the other C6000 DSP platform devices.

The DM642 uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 128-Kbit direct mapped cache and the Level 1 data cache (L1D) is a 128-Kbit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of an 2-Mbit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. The peripheral set includes: three configurable video ports; a 10/100 Mb/s Ethernet MAC (EMAC); a management data input/output (MDIO) module; a VCXO interpolated control port (VIC); one multichannel buffered audio serial port (McASP0); an inter-integrated circuit (I2C) Bus module; two multichannel buffered serial ports (McBSPs); three 32-bit general-purpose timers; a user-configurable 16-bit or 32-bit host-port interface (HPI16/HPI32); a peripheral component interconnect (PCI); a 16-pin general-purpose input/output port (GP0) with programmable interrupt/event generation modes; and a 64-bit glueless external memory interface (EMIFA), which is capable of interfacing to synchronous and asynchronous memories and peripherals.

The DM642 device has three configurable video port peripherals (VP0, VP1, and VP2). These video port peripherals provide a glueless interface to common video decoder and encoder devices. The DM642 video port peripherals support multiple resolutions and video standards (e. g., CCIR601, ITU-BT.656, BT.1120, SMPTE 125M, 260M, 274M, and 296M).

These three video port peripherals are configurable and can support either video capture and/or video display modes. Each video port consists of two channels - A and B with a 5120-byte capture/display buffer that is splittable between the two channels.

For more details on the Video Port peripherals, see the TMS320C64x Video Port/VXCO Interpolated Control (VIC) Port Reference Guide (literature number SPRU629).

The McASP0 port supports one transmit and one receive clock zone, with eight serial data pins which can be individually allocated to any of the two zones. The serial port supports time-division multiplexing on each pin from 2 to 32 time slots. The DM642 has sufficient bandwidth to support all 8 serial data pins transmitting a 192-kHz stereo signal. Serial data in each zone may be transmitted and received on multiple serial data pins simultaneously and formatted in a

multitude of variations on the Philips Inter-IC Sound (I2S) format.

In addition, the McASP0 transmitter may be programmed to output multiple S/PDIF, IEC60958, AES-3, CP-430 encoded data channels simultaneously, with a single RAM containing the full implementation of user data and channel status fields.

McASP0 also provides extensive error-checking and recovery features, such as the bad clock detection circuit for each high-frequency master clock which verifies that the master clock is within a programmed frequency range.

The VXCO interpolated control port (VIC) provides digital-to-analog conversion with resolution from 9-bits to up to 16-bits. The output of the VIC is a single bit interpolated D/A output. For more details on the VIC port, see the TMS320C64x Video Port/VXCO Interpolated Control (VIC) Port Reference Guide (literature number SPRU629).

The ethernet media access controller (EMAC) provides an efficient interface between the DM642 DSP core processor and the network. The DM642 EMAC support both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex, with hardware flow control and quality of service (QOS) support. The DM642 EMAC makes use of a custom interface to the DSP core that allows efficient data transmission and reception. For more details on the EMAC, see the TMS320C6000 DSP Ethernet Media Access Controller (EMAC) / Management Data Input/Output (MDIO) Module Reference Guide (literature number SPRU628).

The management data input/output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system. Once a PHY candidate has been selected by the DSP, the MDIO module transparently monitors its link state by reading the PHY status register. Link change events are stored in the MDIO module and can optionally interrupt the DSP, allowing the DSP to poll the link status of the device without continuously performing costly MDIO accesses. For more details on the MDIO, see the TMS320C6000 DSP Ethernet Media Access Controller (EMAC) / Management Data Input/Output (MDIO) Module Reference Guide (literature number SPRU628).

The I2C0 port on the TMS320DM642 allows the DSP to easily control peripheral devices, boot from a serial EEPROM, and communicate with a host processor. In addition, the standard multichannel buffered serial port (McBSP) may be used to communicate with serial peripheral interface (SPI) mode peripheral devices.

## Key Features

High-Performance Digital Media Processor (TMS320DM642)

2-, 1.67-, 1.39-ns Instruction Cycle Time

500-, 600-, 720-MHz Clock Rate

Eight 32-Bit Instructions/Cycle

4000, 4800, 5760 MIPS

Fully Software-Compatible With C64x

VelociTI.2 Extensions to VelociTI Advanced Very-Long-Instruction-Word VLIW) TMS320C64x DSP Core

Eight Highly Independent Functional Units With VelociTI.2 Extensions:

Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle

Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle

Load-Store Architecture With Non-Aligned Support

64 32-Bit General-Purpose Registers

Instruction Packing Reduces Code Size

All Instructions Conditional

Instruction Set Features

Byte-Addressable (8-/16-/32-/64-Bit Data)

8-Bit Overflow Protection

Bit-Field Extract, Set, Clear

Normalization, Saturation, Bit-Counting

VelociTI.2 Increased Orthogonality

L1/L2 Memory Architecture

128K-Bit (16K-Byte) L1P Program Cache (Direct Mapped)

128K-Bit (16K-Byte) L1D Data Cache (2-Way Set-Associative)

2M-Bit (256K-Byte) L2 Unified Mapped RAM/Cache (Flexible RAM/Cache Allocation)

Endianess: Little Endian, Big Endian

64-Bit External Memory Interface (EMIF)

Glueless Interface to Asynchronous Memories (SRAM and EPROM) and Synchronous Memories (SDRAM, SBSRAM, ZBT SRAM, and FIFO)

1024M-Byte Total Addressable External Memory Space

Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)

10/100 Mb/s Ethernet MAC (EMAC)

IEEE 802.3 Compliant

Media Independent Interface (MII)

8 Independent Transmit (TX) Channels and 1 Receive (RX) Channel

Management Data Input/Output (MDIO)

Three Configurable Video Ports

Providing a Glueless I/F to Common Video Decoder and Encoder Devices

Supports Multiple Resolutions and Video Standards

VCXO Interpolated Control Port (VIC)

Supports Audio/Video Synchronization

Host-Port Interface (HPI) [32-/16-Bit]

32-Bit/66-MHz, 3.3-V Peripheral Component Interconnect (PCI) Master/Slave Interface Conforms to PCI Specification 2.2

Multichannel Audio Serial Port (McASP)

Eight Serial Data Pins

Wide Variety of I2S and Similar Bit Stream Format

Integrated Digital Audio I/F Transmitter Supports S/PDIF, IEC60958-1, AES-3, CP-430 Formats

Inter-Integrated Circuit (I2C) Bus

Two Multichannel Buffered Serial Ports

Three 32-Bit General-Purpose Timers

Sixteen General-Purpose I/O (GPIO) Pins

Flexible PLL Clock Generator

IEEE-1149.1 (JTAG) Boundary-Scan-Compatible

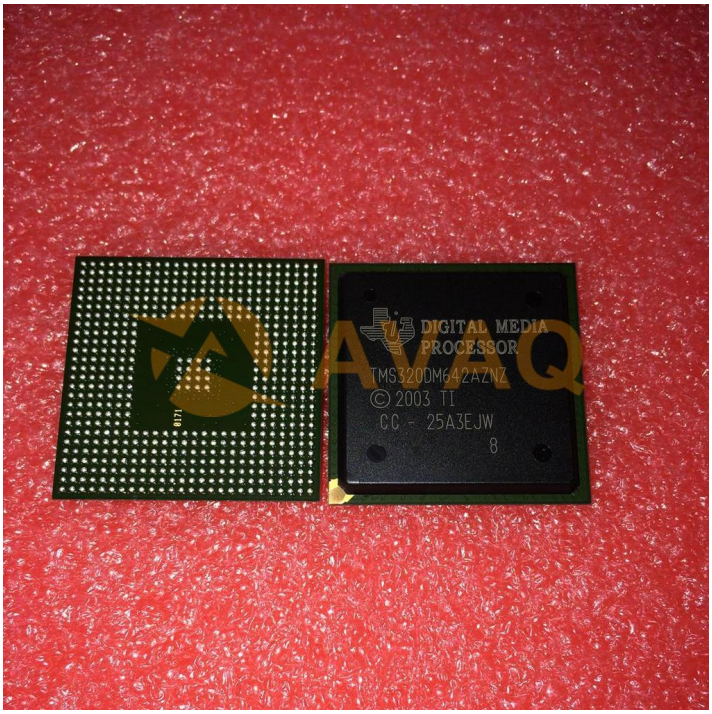
548-Pin Ball Grid Array (BGA) Package (GDK and ZDK Suffixes), 0.8-mm Ball Pitch

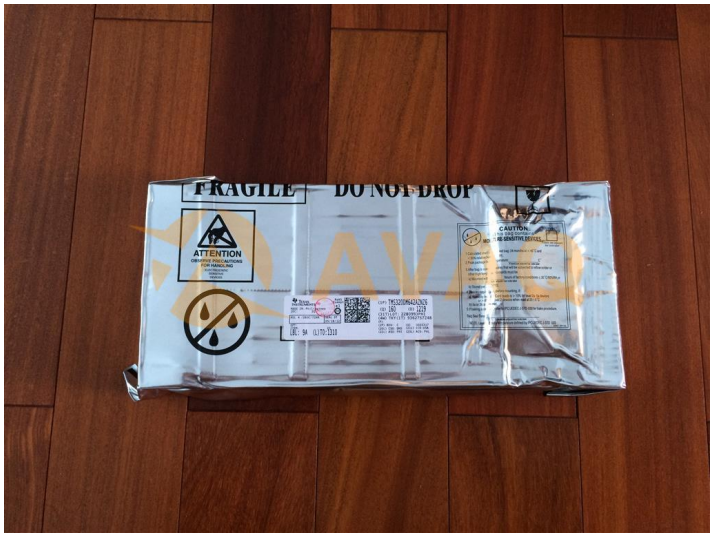
548-Pin Ball Grid Array (BGA) Package (GNZ and ZNZ Suffixes), 1.0-mm Ball Pitch

0.13-µm/6-Level Cu Metal Process (CMOS)

3.3-V I/O, 1.2-V Internal (-500)

3.3-V I/O, 1.4-V Internal (A-500, A-600, -600, -720)




## Recommended For You

**TMS320C31PQA40**

Texas Instruments, Inc

QFP

**TMS320C6726BRFP266**

Texas Instruments, Inc

QFP144

**TMS320DM648ZUTD9**

Texas Instruments, Inc

BGA

**TMS320C203PZ80**

Texas Instruments, Inc

QFP

**TMS320F28027PTT**

Texas Instruments, Inc

LQFP48

**TMS5703137DZWTQQ1**

Texas Instruments, Inc

NFBGA-337

**TMS34010FNL-40**

Texas Instruments, Inc

PLCC

**TMS320C6670ACYPA2**

Texas Instruments, Inc

FCBGA84

**TMS320VC5402APGE16**

Texas Instruments, Inc

LQFP-144

**TMS320DM642AGDKA5**

Texas Instruments, Inc

FCCSP(GDK)

**TMS320C6424ZWT4**

Texas Instruments, Inc

BGA

**TMS320C6711DZDP250**

Texas Instruments, Inc

BGA

**TMS320DM365ZCE30**

Texas Instruments, Inc

BGA

**TMS320DM642AZNZA6**

Texas Instruments, Inc

BGA

**TMS320C50PQ57**

Texas Instruments, Inc

QFP132